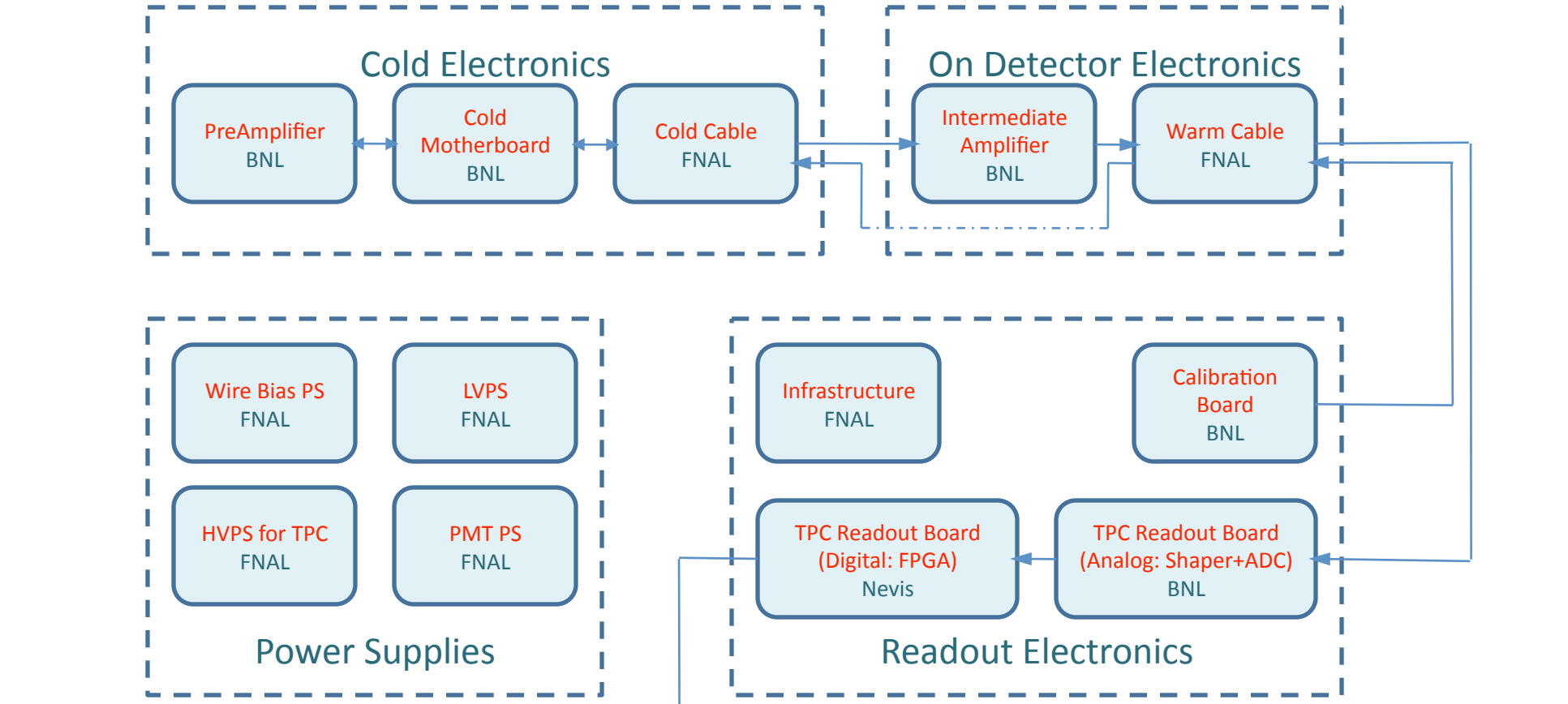
MicroBooNE Electronics

Readout Electronics Layout



- Institutions work together to define the design specification and interface between different parts
- Design will be reviewed/agreed by Electronics WG/Collaboration
- Electronics WG and DAQ WG work together to define the system readout architecture

Electronics Design Parameters

- Needed in CDR
  - Dynamic Range
  - S/N ratio
  - Data rate
  - Sampling rate
  - Pulse width/shaping time
  - ……
- Will be circulated, discussed and agreed

Dynamic Range and S/N Ratio

- Bruce Baller talk in Oct. collaboration meeting
  - MicroBooNE-doc-167-v1
  - 12-bit ADC
  - S/N ratio > 15
  - …

Data Rate Exercises

- Beam Spill Trigger
  - Average rate ~10Hz, peak rate ~15Hz
  - Read out 2.5ms continuously with 5MHz sampling rate
  - Data rate
    - 64-ch TPC readout board
      - Peak: 64-ch x 5MHz x 2.5ms x 16bit x 15Hz = 192Mbps = 24MB/s
      - Average: 64-ch x 5MHz x 2.5ms x 16bit x 10Hz = 128Mbps = 16MB/s
    - Full detector: ~9k channels, 140 TPC readout boards
      - 16MB/s x 140 = 2.24GB/s
- Off Beam Spill
  - Average ~6kHz, ~2k wires, ~100 useful samples on each wire
  - Read out only useful samples after pedestal suppression
  - Data rate
    - 64-ch TPC readout board
      - Peak: 64-ch x 100-sample x 16bit x 6kHz = 614.4Mbps = 76.8MB/s
      - Average: 64-ch x 100-sample x 16bit x 6kHz x 2k/9k = 136.5Mbps = 17.1MB/s
    - Full detector
      - 17.1MB/s x 140 = 2.389GB/s
- Super Nova Trigger
  - Average rate ???
  - Read out 5s continuously with 5MHz sampling rate
  - Data rate
    - 64-ch TPC readout board
      - Peak: 64-ch x 5MHz x 16bit = 5.12Gbps = 640MB/s
      - Provide 4GB local storage using DDR2 SDRAM then impose some dead time to read out at more realistic rate
    - Full detector: ~9k channels, 140 TPC readout boards
      - Peak: 640MB/s x 140 = 89.6GB/s
- Other Trigger…

What does it mean?

- 64-ch TPC readout board
  - Beam Spill Trigger: 16MB/s
  - Off Beam Spill: 17.1MB/s
    - TPC readout board can transfer data to DAQ system over Gigabit Ethernet even in combined mode (16+17.1 = 33.1MB/s)
  - Super Nova Trigger: 640MB/s (peak rate)
    - TPC readout board can transfer data to DAQ system over 6.5Gbps fiber optic link
- But… for Full Detector
  - Beam Spill Trigger: 2.24GB/s
  - Off Beam Spill: 2.389GB/s
  - Super Nova Trigger: 89.6GB/s (peak rate)
  - It is hard for DAQ system to sustain any running mode without significant data reduction
    - D0: peak data flow rate ~500MB/s
    - D0: data written on tape ~25MB/s
  - Data transmission can be done, but we have bottleneck of data processing and data storage

How can we reduce data?

- Beam Spill Trigger
  - Do we need to send all raw data to DAQ system?
    - Yes – reduce beam spill rate by factor of N (for example N=10 to reduce average trigger rate to 1Hz)
    - No – Pedestal suppression
      - Read out only useful samples after pedestal suppression – May lose information
        - » Average ~6kHz, ~2k wires, ~100 useful samples on each wire
        - » Data rate
          - 64-ch TPC readout board
            - Peak: 64-ch x 100-sample x 16bit x 6kHz x 2.5ms x 15Hz = 23.04Mbps = 2.88MB/s
            - Average: 64-ch x 100-sample x 16bit x 6kHz x 2k/9k x 2.5ms x 10Hz = 3.41Mbps = 427kB/s
          - Full detector
            - 427kB/s x 140 = 59.8MB/s
      - Read out all samples with reformatting after pedestal suppression – Without losing any information
        - » Record difference between successive samples , data rate reduced by factor of ~4 (ICARUS: 3.9)
        - » Data rate
          - 64-ch TPC readout board
            - Peak: 192Mbps / 4 = 48Mbps = 6MB/s
            - Average: 128Mbps / 4 = 32Mbps = 4MB/s
          - Full detector
            - 4MB/s x 140 = 560MB/s
  - How to run?
    - Beginning
      - Read out all raw data with reduced beam spill rate
    - Later
      - Read out all samples with reformatting after pedestal suppression

How can we reduce data? (cont.)

- Off Beam Spill
  - We need more sophisticated data reduction techniques after pedestal suppression
    - Hit finding algorithm proposed by Stephan Pordes
      - 80 bits for 8 parameters: wire no., pulse-height, time, pulse-width, rise time, inferred angle, chi-square of fit to single pulse, is there another hit entangled
      - Factor of 20: 100sample x 16bit / 80bit = 20
      - Data rate
        - » 64-ch TPC readout board
          - Peak: 614.4Mbps / 20 = 30.72Mbps = 3.84MB/s
          - Average: 136.5Mbps / 20 = 6.83Mbps = 854kB/s
        - » Full detector
          - 2.389GB/s / 20 = 119.5MB/s
  - How to run?
    - Complimentary to Beam Spill Trigger
    - Combined Mode: Beam Spill Trigger + Off Beam Spill
      - Beam Spill Trigger: Read out all samples with reformatting after pedestal suppression
      - Off Beam Spill : Sophisticated data reduction after pedestal suppression
      - Full detector data rate
        - » 560 + 119.5 = 680MB/s

Data Rate of Readout

- Beam Spill Trigger
  - Read out only useful samples: 59.8MB/s – May lose information
  - Read out all samples with reformatting: 560MB/s
- Off Beam Spill – Read out only useful samples
  - Hit finding algorithm: 119.5MB/s
- Questions:
  - Do we need to read out all samples of beam spill trigger? For how long? (default: 2.5ms)
  - How many cosmic ray events do we need?
  - How sophisticated algorithm can be implemented in FPGA?
  - How sensitive is the data rate affected by the noise?
  - How much CPU time do we need to implement data reduction algorithm in PC?
  - How much data reduction do we need in event builder before tape recording?
  - …